Design and Verification of AMBA APB Protocol using System Verilog

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# Abstract

The Advanced Microcontroller Bus Architecture (AMBA), Advanced Peripheral Bus (APB) protocol stands as a cornerstone in modern System-on-Chip (SoC) designs, serving as the vital link between peripheral components and the central processing unit (CPU). Crafting this interface demands meticulous attention to detail, encompassing the development of an AMBA APB interface that strictly adheres to the protocol's exacting standards. This entails designing and integrating the APB controller, the APB bus interface, and various peripheral modules. Leveraging System Verilog facilitates a modular and adaptable design approach, accommodating diverse data widths, address spaces, and peripheral requisites. In the verification phase, a robust System Verilog testbench is constructed to validate the accuracy of the devised AMBA APB interface. The process entails creating both master and slave functionalities in accordance with the AMBA APB protocol's specifications. The verification environment, constructed with System Verilog, meticulously evaluates the design's capacity for data transfers (read/write), proficient handling of bus arbitration, and adept management of wait states.

**Key Words**: Advanced Microcontroller Bus Architecture, Advanced Peripheral Bus, System Verilog, Central Processing Unit, Testbench.